IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A semiconductor device structure with a substantially planar surface, comprising:

a substrate including at least one recess formed therein; and

a material layer disposed over ~~said~~ the substrate and substantially filling ~~said~~ the at least one recess, ~~said~~ the material layer having a substantially planar surface free of abrasive planarization-induced defects.

2. (Withdrawn and currently amended) The semiconductor device structure of claim 1, wherein ~~said~~ the substrate comprises a semiconductor substrate with a surface and ~~said~~ the at least one recess comprises at least one trench recessed in ~~said~~ the surface of ~~said~~ the semiconductor substrate.

3. (Currently amended) The semiconductor device structure of claim 1, wherein ~~said~~ the material layer comprises a mask material.

4. (Currently amended) The semiconductor device structure of claim 3, further comprising at least one conductively doped region continuous with a surface of ~~said~~ the semiconductor substrate and adjacent ~~said~~ the at least one recess.

5. (Withdrawn and currently amended) The semiconductor device structure of claim 1, wherein ~~said~~ the substrate comprises:

a shallow trench isolation structure including a semiconductor device substrate with a surface and at least one trench formed in ~~said~~ the surface of ~~said~~ the semiconductor device substrate;

and

an insulator layer substantially filling ~~said~~ the at least one trench and covering ~~said~~ the surface of ~~said~~ the semiconductor device substrate.

6. (Withdrawn and currently amended) The semiconductor device structure of claim 5, wherein ~~said~~ the insulator layer includes a nonplanar upper surface with at least one peak located substantially above ~~said~~ the surface of ~~said~~ the semiconductor device substrate and at least one valley located substantially above ~~said~~ the at least one trench.

7. (Withdrawn and currently amended) The semiconductor device structure of claim 6, wherein ~~said~~ the material layer comprises a stress buffer layer that substantially fills ~~said~~ the at least one valley in ~~said~~ the insulator layer.

8. (Withdrawn and currently amended) The semiconductor device structure of claim 1, wherein ~~said~~ the substrate comprises:

a semiconductor device structure including a surface with at least one dual damascene trench formed thereon; and

a conductive layer substantially filling ~~said~~ the at least one dual damascene trench and covering ~~said~~ the surface of ~~said~~ the semiconductor device structure.

9. (Withdrawn and currently amended) The semiconductor device structure of claim 8, wherein ~~said~~ the conductive layer includes a nonplanar upper surface with at least one peak located substantially above ~~said~~ the surface of ~~said~~ the semiconductor device structure and at least one valley located substantially above ~~said~~ the at least one dual damascene trench.

10. (Withdrawn and currently amended) The semiconductor device structure of claim 9, wherein ~~said~~ the material layer comprises a stress buffer layer that substantially fills ~~said~~ the at least one valley in ~~said~~ the conductive layer.

11. (Currently amended) The semiconductor device structure of claim 1, wherein ~~said~~ the substrate comprises a stacked capacitor structure and ~~said~~ the at least one recess comprises at least one container recessed in an insulator layer of ~~said~~ the stacked capacitor structure.

12. (Currently amended) The semiconductor device structure of claim 11, wherein ~~said~~ the material layer comprises a mask material, ~~said~~ the mask material substantially filling ~~said~~ the at least one container.

13. (Currently amended) The semiconductor device structure of claim 12, wherein mask material covering a surface of ~~said~~ the insulator layer has a thickness of less than a depth of ~~said~~ the at least one container.

14. (Currently amended) The semiconductor device structure of claim 12, wherein mask material covering a surface of ~~said~~ the insulator layer has a thickness of less than about half a depth of ~~said~~ the at least one container.

15. (Currently amended) A semiconductor device structure with a substantially planar surface, comprising:

a substrate including at least one recess formed therein; and

a material layer disposed at least partially over ~~said~~ the substrate so as to at least partially fill ~~said~~ the at least one recess, ~~said~~ the material layer having a substantially planar surface substantially free of abrasive planarization-induced defects.

16. (Currently amended) The semiconductor device structure of claim 15, wherein at least one region of ~~said~~ the substrate is exposed through ~~said~~ the material layer.

17. (Currently amended) The semiconductor device structure of claim 15, further comprising:

at least one intermediate layer between ~~said~~ the substrate and ~~said~~ the material layer, at least one portion of ~~said~~ the at least one intermediate layer at least partially filling ~~said~~ the at least one recess.

18. (Currently amended) The semiconductor device structure of claim 17, wherein at least one region of ~~said~~ the at least one intermediate layer is exposed through ~~said~~ the material layer.

19. (Currently amended) The semiconductor device structure of claim 17, wherein ~~said~~ the at least one intermediate layer comprises at least one of a mask material, an insulative material, and a conductive material.

20. (Currently amended) The semiconductor device structure of claim 15, wherein ~~said~~ the material layer has a thickness that is less than a depth of ~~said~~ the at least one recess.